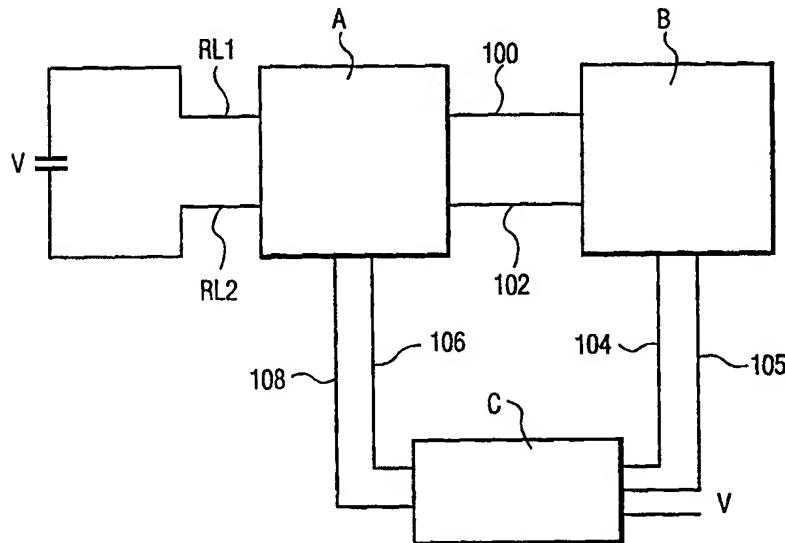




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(54) Title: VOLTAGE REGULATION SCHEME FOR POWER SUPPLY HAVING A VOLTAGE-FED INVERTER



(57) Abstract

A power supply is disclosed, including a resonant circuit having an output voltage and a current oscillating therethrough, and a voltage-fed half-bridge inverter producing a source voltage at an output coupled to the resonant circuit, the inverter responsive to a driving signal. A driving circuit has a first input representing the sensed current oscillating through the resonant circuit, a second input representing the output voltage, and a reference voltage. The driving circuit includes compensation circuitry maintaining output voltage at the reference voltage and commanding a phase shift angle, and phase-shifting circuitry producing the driving signal based on a phase-shift of the sensed current, the amount of phase shift commanded by the compensation circuitry.

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VOLTAGE REGULATION SCHEME FOR POWER SUPPLY HAVING A VOLTAGE-FED INVERTER.

The invention generally concerns power supplies and lighting ballasts, and more particularly to voltage regulation for zero-voltage-switched (ZVS) inverters.

Electronic lamp ballasts include inverters to provide a high frequency substantially square wave voltage output to a load. The load typically includes a resonant circuit and lamps. A typical inverter circuit includes power switching circuitry involving transistors to convert a DC input to a desired high frequency AC output.

A control circuit, such as disclosed in U.S. Patent No. 4,952,849 to Fellows et al. for driving the switching circuitry of voltage-fed inverter, senses current flowing through the load to control the switching circuitry. The switches are turned on so as to minimize damage and losses thereto during transition and is commonly referred to as zero-voltage switching (ZVS). The switching technique minimizes voltage across the switch as the switch is being turned on.

The switching frequency of the inverter is typically above the resonant frequency of the resonant circuit, that is, to maintain the resonant circuit in an inductive mode. More generally, in the zero-voltage switching scheme, it is critical to maintain the circuit in an inductive mode when transitioning between the power switches, regardless of the load type. Otherwise, large power losses and damage to the components within the circuit can result.

One commonly used method to achieve zero-voltage switching is to maintain the switching frequency higher than the resonant frequency, as described in Steigerwald, "A Comparison of Half-Bridge Resonant Converter Topologies," IEEE Transactions on Power Electronics, April 1988, pp. 174-181, incorporated by reference herein. This frequency-based scheme can be easily implemented using voltage controlled oscillators (VCO). However, a critical requirement of such control method is that prior knowledge of the resonant frequency is needed to determine the frequency sweeping region. In simple applications, for example, in LC resonant inverter-based power supplies and electronic ballasts with a single lamp, when the maximum gain frequency does not change significantly during the load and line changes, the frequency-based control method operates successfully.

However, in some cases, the characteristics of the resonant circuit can change rapidly with lamp loads, bus voltage, ambient conditions or aging of the components. Such changes can affect the operating mode of the resonant circuit. Simple frequency based control methods may be unable to adapt to the new frequency-sweep region and therefore be unable to 5 maintain zero voltage switching.

The circuit of Nalbant, "A New and Improved Control Technique Greatly Simplifies the Design of ZVS Resonant Inverters and DC/DC Power Supplies," Proceedings of IEEE Applied Power Electronics Conference, March 1995, pp. 694-701, achieves zero voltage switching by increasing the operating frequency above the resonant frequency.

10 Switching occurs by setting thresholds on the current flowing in a loading matching network. When one of these thresholds is crossed, switching occurs in the inverter. This approach has the disadvantage that threshold values must be chosen and set, and complex logic must be implemented. If the current values experience large fluctuations, the threshold may not be crossed and a correct switching cycle may be missed, or the wrong operating frequency may 15 result. Here, the inductor current information is not further used for output regulation.

Accordingly, it is the object of the invention to provide various voltage regulation methods in a zero-voltage switching scheme for a power supply or ballast having a voltage-fed inverter which overcomes the above mentioned disadvantages of the prior art.

20 A high frequency resonant power supply is disclosed which includes a resonant circuit having an output voltage and a current oscillating therethrough, a voltage-fed half-bridge inverter producing a source voltage at an output coupled to the resonant circuit, the inverter responsive to a driving signal. The power supply further includes a novel driving circuit producing the driving signal.

25 The driving circuit has compensation circuitry regulating the output voltage with respect to a reference voltage and commanding a phase shift angle. Phase-shifting circuitry in the driving circuit applies a phase-shift to the sensed current, and the amount of phase shift is commanded by the compensation circuitry.

30 The phase-shifting circuitry applies the positive phase angle shift to the sensed current input such that the voltage at the output of the inverter is leading the sensed current input with the predetermined positive phase angle. The driving signal may actuate a switch in the inverter when the phase-shifted sensed current signal crosses zero. The phase shifting circuitry preferably includes an all-pass filter.

In a preferred embodiment, the driving circuit includes a filter for suppressing a low frequency component of the sensed current flowing through the resonant circuit. The power supply may further include a load, wherein the load is a discharge lamp.

5 In a preferred embodiment, the driving circuit includes a hysteresis control with respect to the sensed current signal. The hysteresis control is used to establish the switching times. The hysteresis relation is so designed that the zero-voltage switching is always achieved at each switching time, regardless of the load situation.

A method for switching a power supply is also disclosed which includes the steps of providing a resonant circuit having a current oscillating therethrough; providing an 10 inverter responsive to a driving signal and producing a voltage at an output coupled to the resonant circuit; sensing the current oscillating through the resonant circuit; applying a phase angle shift to the current; applying a driving signal to the inverter based upon the phase-shifted current.

15 In a preferred embodiment, the method further includes the step of filtering the sensed current signal to suppress low frequency components prior to applying the phase angle shift. In the method for switching a power supply, the step of applying a driving signal to the inverter preferably includes actuating a switch in the inverter when the phase-shifted current crosses zero.

20 A method for switching a power supply is also disclosed which includes the steps of providing a resonant circuit having a current oscillating therethrough; providing an inverter responsive to a driving signal and producing a voltage at an output coupled to the resonant circuit; sensing the current oscillating through the resonant circuit and producing a sensed current signal proportional to the current; applying a phase angle shift to the sensed current signal and producing a phase-shifted signal; and applying a driving signal to the 25 inverter based upon zero-crossing points of the phase-shifted signal.

It is an object of the invention to provide a voltage regulation method using a phase shift of the signal, for example, for the signal applied to the resonant inverters.

30 It is an object of the invention to provide a voltage regulation method using a level shifted control reference compared with the sensed current signal, for example, for the signal applied to the resonant inverters.

It is a further object of the invention to provide a voltage regulation method, using a level-shifted control reference multiplied with the sensed current signal, for example, for the signal applied to the resonant inverters.

It is an object of the invention to produce an improved zero-voltage switching scheme which employs a phase-shifting technique in timing the switching cycles in the inverter.

It is another object of the invention to provide a switching scheme which does not require prior identification of the resonant frequency.

5 It is a further object of the invention to provide a general switching scheme which is applicable to resonant circuits of second order and higher.

It is yet another object of the invention to provide a switching scheme which does not require complex threshold logic for the timing of the switches.

10 These and other objects, features and advantages of the invention will become apparent with reference to the accompanying drawings and the following detailed description and claims.

FIG. 1 is a block diagram of the power supply in accordance with an exemplary embodiment of the subject invention;

15 FIG. 2(a) is a curve illustrating normalized frequency $A(f)$ as a function of the phase angle f between current and voltage;

FIG. 2(b) is a curve illustrating circuit voltage gain as a function of the phase angle between current and voltage;

20 FIG. 3 is time plot of the current flowing through the resonant circuit and voltage;

FIG. 4(a) is a plot of the relationship between voltage gain and frequency for a lamp load;

FIG. 4(b) is a plot of the relationship between phase angle and frequency for a lamp load;

25 FIG. 5 is a plot of the relationship between voltage gain and phase angle for a lamp load;

FIG. 6 is plot of the hysteresis function to achieve the switching cycling of Fig 3;

FIG. 7 is a schematic diagram of the inverter and the power supply;

30 FIG. 8 is a block diagram of the power supply, illustrating the particular functions of the driving circuit;

FIG. 9 is a schematic diagram of a portion of the driving circuit, illustrating the current signal amplifier, the high-pass filter, gain control, phase-shift circuitry;

FIG. 9A is a schematic diagram of the voltage feedback and regulation circuitry;

FIG. 10 is a partial schematic, partial logic diagram of a portion of the driving circuit, illustrating the wave-shaping and PWM functions;

5 FIG. 10A is partial block diagram, partial schematic diagram of the timer circuit of Fig. 10;

FIG. 11 is a schematic diagram illustrating the start-up circuitry;

FIG. 12 is a schematic diagram illustrating the initiation frequency sweep function associated with start-up;

10 FIG. 13 is a schematic diagram illustrating the bridge driver circuitry;

FIG. 13A is a schematic diagram illustrating the functions of the driver IC;

FIG. 14 is a time plot of the current flowing through the resonant circuit, the phase-shifted signal, and the switching sequence of the switches;

15 FIG. 15 is a schematic diagram of an alternative embodiment of the subject invention;

FIG. 16 is a schematic diagram of a second alternative embodiment of the subject invention; and

FIG. 17 is a schematic diagram of a third alternative embodiment of the subject invention;

20 The power supply circuit shown in Fig. 1 includes a voltage source V, inverter circuit A, resonant circuit and load B, and driving circuit C which controls inverter circuit A. Voltage source V is a direct current voltage source supplying inverter circuit A via lines RL1 and RL2. Alternatively, an AC voltage source may be substituted in conjunction with a rectifier circuit, which may further include power factor correction. Inverter circuit A is of the voltage-fed half-bridge topology, and is under control of the driving circuit C. Resonant circuit B receives the substantially square wave output of inverter circuit A on lines 100 and 102 into a substantially sinusoidal lamp current. In the exemplary embodiment, the load is a parallel-loaded lamp system.

30 The driving circuit C receives a voltage signal proportional to the current flowing through the resonant circuit B via line 104. Phase shifting circuitry is present in driving circuit C to shift the sensed current signal by a predetermined phase angle. The phase angle δ may be an input to the system or the output of a voltage compensator, e.g. circuit 270. This reference voltage V_{ref} could also be used as a dimming interface in dimmable lamp

systems. The driving signals 106 and 108 to the inverter are based upon this phase-shifted current signal to provide zero-voltage switching and to control inverter circuit A.

The voltage across the load is present on line 105. This signal is used to provide voltage feedback and regulation. Voltage across the load is compared with a reference voltage V_{ref} in driving circuit C as will be described below.

As is known in the art, the normalized frequency A (i.e. $A = a_s/a_r$, where a_r is the resonant frequency and a_s is the operating frequency) and the quality factor Q uniquely determine the second order circuit characteristics. Thus when the quality factor Q is known, the power source frequency A is traditionally used to control the circuit voltage gain A, since $A = f(A, Q)$. Likewise, the input phase angle f between the voltage and current is a function of the operating frequency, i.e. $f = g(A, Q)$. Thus, for a particular quality factor Q we can find an inverse function for frequency, i.e. $A = h(f)$, in the region where the relation between $f = g(A, Q)$ and A is one-to-one. That is, there is a unique solution in which there is one operating frequency for a particular phase angle. The function in this region is plotted in Fig. 2(a).

Substituting the function A(f) into the known expression for circuit voltage gain A(A) results in a relation A(f), which is plotted in Fig 2(b). Therefore, it is possible to regulate the voltage gain A by using the input phase angle f as a control variable.

As described above, there may be a region in which the relation between phase angle f and frequency A is not one-to-one. Thus, for each chosen f, there may be two or more corresponding frequencies. In order to use the phase shift based control in this region, some measures need to be taken to eliminate either the higher frequency branch or the lower frequency branch. Properly designed filters could be used to serve this purpose, as will be described hereinbelow.

In the implementation of the phase shift based control method, the input phase angle f is driving variable and the source frequency is a derived variable along the curves of Figs. 2(a) and 2(b). An open or closed loop system may be used to implement the phase shift based control scheme.

The bridge type inverter output voltage V_s and the current flowing through the resonant circuit i_L are plotted in the time domain in Fig. 3. The phase angle between the voltage V_s and current i_L is f. The phase angle is defined as $f = 2X(t_f/T_s)$, where t_f is such that $i_L(t_f) = 0$, or the zero current crossing point. By sensing the current signal i_L , processing it with a driving circuit and driving the switches of the inverter, a feedback loop is implemented.

With the circuit topology as in Fig. 7, the voltage gain and the phase angle are plotted versus frequency, see Figs. 4(a) and 4(b), for a lamp load configuration. As described

above, the inverter is favorably operated in the higher frequency branch of the voltage gain frequency curves where the input phase angles are kept positive.

When the load changes, the steady state operating point shifts in order to achieve a regulated output voltage. For a step change in the load, the steady state operating 5 point shifts from one curve to another. In order to regulate the output voltage to a constant value, the corresponding frequency has to be changed. In some cases, the relationship is strongly dependent on the load that the voltage gain / frequency curves for different loads are widely spread, e.g. when the lamp resistance changes due to the dimming operation.

Traditional frequency based control method has difficulty in reaching the proper operating 10 points during fast load change. Moreover, the power switches in the prior art system tend to lose zero-voltage switching during the process.

The voltage gain is plotted versus phase angle in Fig. 5 based on the relationships of voltage gain to frequency in Fig. 4(a) and phase angle to frequency in Fig. 4(b). When the load changes, the voltage gain versus frequency and the input phase angle 15 versus frequency curves will change accordingly. At a first load condition illustrated by curve LO1, the circuit operating point is at operating frequency f_A , voltage gain V_A and phase angle f_A . The phase angle f_A is positive which indicates the zero-voltage-switching condition for all bridge power switches, i.e. Q1 and Q2. When the load changes abruptly, the circuit characteristics change from curve LO1 to LO2 in Figs. 4(a), 4(b) and 5. The traditional 20 frequency sweeping based control method will move the operating point to an intermediate point having the same initial operating frequency f_A , but new voltage gain V_B and new phase angle f_B before sweeping to the new steady state point at operating frequency f_B , voltage gain V_B and phase angle f_B . At this intermediate point, the phase angle f_B is negative. Therefore, the zero-voltage switching condition is not maintained, which in turn may cause switch failure. 25 By implementation of the phase angle shift control scheme, the phase angle can be adjusted accordingly such that the output voltage is regulated, as illustrated in Fig. 5. Here, the operating frequency is adjusted indirectly. The phase angle change region remains at the positive side. This implies that the inductive mode is always maintained, even during the transient process. More specifically, in order to maintain a constant voltage gain, the values 30 M1 and M2 of Fig. 3 need to be adjusted as described below.

A proposed relation H for the driving circuit is shown in Fig. 6. The trigger points a and b in Fig. 6 correspond to the points a and b in Fig. 3. The variables M1 and M2 are selected as the hysteresis threshold of Fig. 6, such that $i_L(t=0)=M1$ and $i_L(t=DT_s)=M2$ in Fig. 3. The time duration from the zero current crossing point $i_L=0$ to the trigger point a when

i_L is decreasing is $-t_1$, and the duration from the zero current crossing point when i_L is increasing to the trigger point b is $-t_2$. Thus, the switching in the inverter occurs when the current i_L crosses the values M1 and M2.

The quantities of M1, M2 and $-t_1$, $-t_2$ are related and are a function of the input 5 phase angle f. As M1 or M2 is decreased, the switching threshold is reached sooner. Consequently $-t_1$ or $-t_2$ decreases, and switching frequency increases. Likewise, the converse is typically true that an increase in M1 or M2 results in a decrease in frequency.

In the power inverters, the load may change during the operation. If H is fixed, a new stable point may be reached as long as some necessary and sufficient conditions are 10 met. The power inverter characteristics (oscillating frequency, gain, phase angle, etc.) change with the load. If such a change is not favorable to certain performance objectives, necessary control scheme is needed. In this case, we can control the operation by adjusting the hysteresis H in Fig. 6. The control variables could be M1 and M2, which are used to effectively change the phase angle f. The hysteresis is implemented in the preferred embodiment as a comparator 15 circuit as illustrated in Fig. 10, although the other methods are contemplated as within the scope of the invention. It is likewise contemplated that the hysteresis control may be implemented in conjunction with the phase-shift circuitry. For example, the sensed current signal may be phase-shifted and subsequently the phase shifted signal is used to create a driving signal by use of a hysteresis function as above.

20

The Inverter Circuit

Turning now to FIG. 7, inverter circuit A includes a pair of switches Q1 and Q2 which are arranged in a half-bridge configuration and convert the DC voltage from voltage source V to a high-frequency substantially square wave AC output signal across the inverter 25 outputs, under the control of driver circuit C. Although the present embodiment is described with respect to a half-bridge inverter having a pair of switches, the switching scheme described herein is applicable to a full bridge topology having four switches. In such a configuration, the switches would be controlled in pairs rather than individually.

The switches Q1 and Q2 are preferably MOSFETs, although it is contemplated 30 that BJTs could also be used as the power switches. Switch Q1 is effectively connected in parallel with diode D1, which could be the body diode if MOSFETs are used. A snubber capacitor may also be connected in parallel with switch Q1, which may include the junction capacitor contingent to switch Q1. Similarly, switch Q2 is connected in parallel with diode D2. Likewise, a snubber capacitor may also be connected in parallel with switch Q2, which may

include the junction capacitor contingent to switch Q2. The drain of switch Q1 is connected via the rail RL1 to the output from the voltage source V. The source of the switch Q1 is connected to the drain of switch Q2. The control gate of switch Q1 is connected via control line 108 to a respective gate controller terminal of driving circuit C via a parallel arrangement 5 of a resistor R10 and a diode D10. The anode of diode D10 is connected to the control gate of the switch Q1. The diode D10 provides rapid evacuation of charges from the control gate to enhance switching speed. The control gate of switch Q2 is similarly connected to a gate controller terminal of driving circuit C through control line 106. A similar parallel arrangement exists for switch Q2 with resistor R12 and diode D12. This particular 10 arrangement has been implemented in conjunction with MOSFET switches Q1 and Q2. A different gate drive would be implemented for bipolar transistor switches, which is within the scope of the present invention.

Line 100 connects the midpoint I between the source of the switch Q2 and the drain of the switch Q1 to one end of the blocking capacitor Cbk. Capacitor Cbk blocks DC 15 components of the inverter output voltage generated at node I. Line 112 connects the midpoint I via resistor R14 to driving circuit C, as will be described below. Line 102 is connected to the drain of switch Q2. Line 100 and line 102 serve as the output of inverter circuit A. The output of inverter A is a substantially square wave voltage source.

20 Resonant Circuit

With continued reference to Fig. 7, The resonant circuit B shapes the voltage and current waveforms to the load, such as a parallel loading of an instant start fluorescent lamps L1, which is in series with ballasting capacitors CL1.

The resonant circuit B includes resonant inductor Lr connected in series with 25 the blocking capacitor Cbk via line 100. Resonant capacitor Cr is connected in parallel with a primary winding of isolation transformer T1.

Due to the high Q filtering action of the resonant circuit B on the square wave voltage output of the inverter circuit A, the current flows with a substantially sinusoidal waveform. This current is sensed by the voltage drop on line 102 across R20, having a small 30 resistance. The sensed current signal on line 104 serves as a input to driving circuit C as will be described below.

Inverter Controller Circuit

Fig. 8 illustrates, in block diagram form, the components of driving circuit C. Current sensing circuit 200 senses the voltage drop across RS1. High-pass filter 204 is used to filter one of the frequency components of the sensed current. The higher frequency component corresponding to the operating frequency is permitted to pass, but lower frequency signal components are suppressed from the current signal. As a result, the inverter is forced to operate in the higher frequency branch of the voltage gain frequency curves, where the input phase angles are kept positive. Automatic gain control 206 is utilized to control the amplitude of the signal so as to avoid saturating circuit components. Phase shifting circuitry 208 provides a phase shift of f to the input signal. The amount of phase shift f applied by phase shifting circuitry 208 is determined within a closed loop feedback scheme. The phase shift control voltage is the controlled output on line 105. The feedback path consists of feedback gain 250. The reference voltage V_{ref} is preselected and compared with the actual voltage in compensator 270, which provides an actuating signal on line 150. The signal on line 150 is used to control the amount of phase angle shift to regulate output voltage. Wave shaping circuitry 210 is triggered by the zero-crossing points of the phase-shifted current signal. Pulse width modulation 212 produces the switch pulses, and gate driver 216 controls the timing of the switches and corresponding duty cycles. Start-up logic 214 transitions operation of the lamp from start-up to the steady state operating condition.

Turning now to FIG. 9, current sensing circuit 200, a differential amplifier, 20 senses the voltage drop across R20. R22, R24, R26, R28 and R30 are connected to op-amp 202, such as LT1122, to provide output voltage signal on line 106 which is proportional to the current in the resonant circuit B. The signal is substantially sinusoidal at the operating frequency, and normally has lower frequency components. High pass filter 204 receives the signal of the sensed current. Capacitor C10 and resistor R32 are selected to suppress this low frequency component of the current signal. The present invention is applicable to resonant circuits of higher order as well. Therefore, there may be a plurality of low frequency components to the oscillating current signal which are suppressed by filter 204.

Automatic gain control 206 is provided on the output from high pass filter 204, which prevents the sensed current signal from saturating the components of the following 30 circuitry. A pair of inverting op amps 220 and 222 are used to scale the signal magnitude and provide positive gain factor. The ratio of external resistors R34/R36 for op amp 220 and R38/R40 for op amp 222 are selected to scale the signal. Because the amplitude of the signal flowing through the circuit may fluctuate, an automatic gain controller 224 is used to maintain the signal within a given range. Automatic gain controller 224 is followed by op-amp 226. The

gain is controlled by voltage controlled resistor, such as JFET T1, in parallel with impedance R42. The gate of JFET T1 is connected to the feedback path consisting of impedance R44, diode D20, zener diode D22 and RC circuit consisting of resistance R46 and capacitance C12. An additional inverting amplifier 226 further scales the signal by selection of resistors R52 and R54.

Phase shifting of the sensed signal is performed by the phase-shifting circuitry 208, which includes the pair of all-pass filters 228 and 230 in series. The all-pass filters incorporate op-amps such as LT1122. As is known in the art, such filters provide a loop gain of 1 but provide a predetermined phase angle shift to the signal passing therethrough. The 10 amount of phase shift angle is determined by the control voltage in line 150, which is the output of the voltage compensator 270.

The circuitry of the present invention allows the phase angle to be a driving variable. As described above, the application of a positive phase angle to the sensed current signal ensures zero-voltage switching when the zero-crossing points of the phase shifted signal 15 is used as a control signal for turning on the switches in the inverter circuit A. Ideally, the selection of any positive phase angle will assure zero-voltage switching. In practice, however, due to the output junction capacitance of the MOSFETs used for switches Q1 and Q2, there is a minimum phase angle requirement.

The phase angle may be implemented by an open loop or a closed loop based 20 scheme. In the open loop scheme (not shown), the amount of phase shift may be preselected by selecting the amount of resistance R56 and R58 in parallel with the capacitors C14 and C16, respectively, to the non-inverting input in all-pass filters 228 and 230, respectively. Such resistors R56 and R58 may be at ground potential (not shown). Alternatively, potentiometers 25 (not shown) or voltage controlled devices, such as JFETs T10 and T12, may be used in the closed loop based scheme. The present circuit is shown with two all-pass filters, although a greater or fewer number of filters is contemplated. The optimum phase shift may be determined empirically from the circuit characteristics, such as the capacitance of the snubbing capacitors in parallel with switches Q1 and Q2 if used in the circuit, or the current.

In order to regulate the output voltage, a closed loop scheme may be 30 implemented including voltage compensation circuitry, as illustrated in Fig. 9A. As described above, voltage regulation is possible by using the phase angle. With such a scheme, output voltage regulation may be performed by sensing the output voltage across the load. In the present embodiment, voltage across the load is present on line 105. The signal is rectified by diode D30 and scaling is applied by resistors R80 and R82 in series. Filtering of the signal is

provided by the filter 252, including series resistors R84 and R86 in parallel with capacitor C40. The signal is amplified by noninverting amplifier 254, consisting of op-amp 256, with the ratio of resistance R88/R90 chosen to provide the proper gain.

The signal on line 140 subsequently is acted upon by the voltage compensator

5 circuit 270. The reference voltage is applied to op-amp 272 at the noninverting terminal.

Reference voltage V6 may be applied directly. Preferably, a voltage divider including R92 and potentiometer R94 may be used to provide a variable reference voltage. The op-amp 272 may be configured as a PI regulator, with the feedback path having a parallel combination of capacitor C42 with resistor R96 and capacitor C44 in series. The output of the PI regulator
10 encounters resistor R98 and parallel combination of diode D40, zener diode D42 and capacitor C46, which limit the dynamics of the signal in order to avoid saturating the components of the circuitry, namely JFETs T10 and T12, as will be described below.

With continued reference to Fig. 9, output signal of compensator 270 is present

on line 150. JFETs T10 and T12 are in series with resistors R58 and R56 respectively. Line

15 150 is connected at the gates of T10 and T12 and thereby controls the resistance at the

noninverting terminals of the op-amps 228 and 230. Thus the phase angle shift f may be

precisely controlled.

Since the output voltage is a function of the operating frequency or the phase

angle, output voltage regulation may be achieved by adjusting the phase angle in order to

20 produce the desired output voltage. This scheme may find application in light dimming

ballasts.

Following the phase shifting of the signal, the wave shaping circuitry 210

provides timing for the initiation of the switching as will be described below. Filter including

capacitor C18 shapes the signal, and buffer 231 is a voltage follower interposed to provide a

25 low output impedance and isolation from the input. The output of buffer 230 is on line 119.

Noninverting amplifier 232 (Fig. 10) includes op-amp 234, and external resistors R60 and R62

are selected to scale the voltage. Filter 236 includes resistor R64 and C20.

With continued reference to Fig. 10, the switching signal is generated by a

timing circuit, such as standard 555 timing IC 300, an exemplary circuit being produced by

30 Motorola for example, the specifications of which are incorporated by reference herein and

illustrated in Fig. 10A. Timer 300 is configured in the monostable mode wherein the driving

signal is triggered to the "on" state by the zero-crossing of the phase-shifted current signal.

Comparator 310 converts the substantially sinusoidal analog voltage signal from filter 236 to a square wave sequence which corresponds to the zero-crossing point of the shifted current

signal. The comparator converts this zero-crossing point to set the leading edge of the switching pulse.

Applied voltage V1, in combination with resistors R66 and R68 and diode D30, provide a proper scaling to the signal to the inverter I1. High pass filter 238, including

- 5 capacitor C22 and resistor R70 and diode D32 in parallel, and inverter I2 further shape the signal on line 120, which is connected to the trigger input (pin 2) of the timer 300. The threshold terminal (pin 7) and the discharge terminal (pin 6) are connected together in this mode. The control voltage at pin 5 is preset to a constant value by a voltage divider with resistors R72 and R74. The output signal is present on line 122 from output terminal (pin 3).
- 10 Output signal on line 122 from timing circuit 300 and output on line 123 from start-up circuit 320 pass through OR gate 214 which acts as an electronic switch.

As illustrated in Figs. 11-12, start-up circuit 320 provides the function of initial frequency sweeping for lamp ignition. Start-up circuit 210 includes voltage controlled oscillator (VCO) 312, single pulse flip-flop 314 in Fig. 11 and a DC voltage sensing and scaling circuit 316 (Fig. 12). VCO 312 is preferably voltage-to-frequency converter AD654 produced by Analog Devices of Norwood, Massachusetts, the specifications of which are incorporated by reference herein, although any suitable VCO is contemplated for use in this circuit. The start-up process is described as follows. In Fig. 11, before the DC bus voltage V is fully built up, the voltage in line 130 is low and the output pin Q of the flip flop 314 is high.

20 VCO 312 starts to operate at high frequency region f_{start} which leads to a high frequency square wave signal in line 123. The output voltage of the resonant circuit B is low due to the high frequency operation and lower DC bus voltage V.

When the DC bus voltage is increased to a preset threshold, the output voltage of comparator 318 in Fig. 12 is set to low. This in turn triggers the flip flop 320 and sets the voltage to high at line 130. Effectively, in Fig. 11, the voltage input at control voltage terminal (pin 4) of VCO 312 is reduced gradually. Correspondingly, the output frequency produced by VCO 312 is reduced. This process completes the frequency sweeping from high frequency f_{start} to lower operating frequency f_{op} . Correspondingly, the resonant circuit output voltage to the lamps L1, L2, L3 and L4 is gradually increased until the lamps are ignited. After the lamps are operating, the processed current signal in line 122 triggers the flip-flop 314 and the output signal on line 123 is blocked by using the OR gate 322. Subsequently, the power supply in Fig. 8 operates at a self-oscillating frequency with predetermined phase angle f.

Turning now to Fig. 13, the signal 124 is inverted at logical inverter I6. The signal subsequently passes to the "in" terminal at gate driver 330, such as half-bridge driver

integrated circuit IR2111 produced by International Rectifier, El Segundo, California, the specifications of which are incorporated by reference herein and illustrated at Fig. 13A. With continued reference to Fig. 13, gate driver 330 includes logic to convert a single square wave input signal, such as that on line 124, into two separate driving signals on lines 108 and 106
5 which control switches Q1 and Q2, respectively. Gate driver 330 may be configured to produce signals 108 and 106 such that a blanking time exists in which neither Q1 nor Q2 conduct.

The waveforms produced by the above-described circuit are represented in the time plot illustrated in Fig. 14. The current flowing through the resonant circuit B is
10 represented on the plot by signal 500. Within driving circuit C, this signal corresponds to the voltage signal on line 114, which is proportional to the current and has been filtered of lower frequency components by high-pass filter 204 (See, Figs. 8-9). As described above, the signal on line 114 passes through automatic gain control 206 and phase-shifting circuitry 208. The phase shifted signal 502 corresponds to the output of phase-shifting circuitry 208 on line 118
15 (See, Fig. 9). The phase-shifted signal 502 is phase-shifted by an amount 504 corresponding to f as described above. The zero-crossing point of signal 502 is used as the reference to control switching. Thus, at the zero-crossing point 508, switch Q1 is turned off, as indicated by line 510 (solid line) and switch Q2 is turned on, as indicated by line 512 (dot-dash line). The figure illustrates that Q2 is turned on at the same time that Q1 is turned off. A blanking time 514 is
20 ordinarily provided by driver 304 such that Q1 and Q2 are both off for a brief period of time. When the system load changes, the voltage compensator 270 in Fig. 9(a) generates appropriate control signal in line 150 of Fig. 9(a), which is effectively connected to the gates of JFETs T10 and T12 in Fig. 9. As a result, the phase angle f is adjusted accordingly such that the output voltage is regulated.

25 An alternative embodiment is shown at Fig. 15. A controllable hysteresis threshold may be implemented as described above with respect to Figs. 3 and 6. Comparator 310 converts the substantially sinusoidal analog voltage signal from op-amp 226 to a square wave sequence which corresponds to the crossing points of the current signal with the threshold settings M1 and M2. The logic selection unit 320 converts the basic unipolar DC
30 signal in line 150 into a bipolar DC signal at line 151, which serves as the threshold value M1 and M2 as in Fig. 3. The comparator detects these crossing points to set the leading edge of the switching pulse. In such an implementation, the converted voltage sensing on line 150 of Fig. 9A and the filtered current signal on line 116 of Fig. 9 are inputs to the comparator. In particular, the voltage signal 150 via a logic selection unit 320 would be fed into the non-

inverting input of the comparator 310 and the current signal 116 would be fed into the inverting input of the comparator 310. It is also contemplated that the phase-shifting circuitry be applied as shown in Figs. 9 and 9A to the current signal and a hysteresis control be used in conjunction therewith to adjust the driving signal and consequently the switching times. It is 5 further contemplated that a Schmitt trigger or other voltage level detector may be used in the circuit as an alternative to the comparator 310.

Figs. 16 and 17 illustrate second and third alternative embodiments of the subject invention. In these embodiments, the hysteresis threshold, e.g. M1 and M2, is fixed, rather than controllable. Thus, a constant voltage V10 and V12, through a logic selection unit 10 320, is applied to the non-inverting input of comparator 310 in the embodiments of Fig. 16 and Fig. 17, respectively. It is also contemplated that voltages V10 and V12 may be variable. The circuits are substantially as described above with respect to the previous embodiments, with the differences noted hereinbelow. In the second embodiment of Fig. 16, the output voltage signal of the voltage compensator 270 on line 150 (Fig. 9A) and the sensed current signal on 15 line 115 (Fig. 9) are multiplied in multiplying IC 360, and the product of the two signals is directed to the inverting input of comparator 310. By doing so, the relative magnitude between the sensed current signal and the thresholds M1 and M2 is changed with reference to Fig. 3. In this case, the thresholds M1 and M2 are fixed while the sensed current signal is multiplicatively scaled up or down controlled by the output signal on line 150 of the voltage 20 compensator 270. Consequently, the switching time $-t_1$ and $-t_2$ are adjusted in Fig. 3. In return, the phase angle f is controlled.

In the third embodiment of Fig. 17, the control voltage signal on line 150 (Fig. 9A) and the sensed current signal on line 115 (Fig. 9) are added via the combination of multiplying IC 370 and op-amp 270. By doing so, the relative magnitude between the sensed 25 current signal and the thresholds M1 and M2 is changed with reference to Fig. 3. In this case, the thresholds M1 and M2 are fixed while the sensed current signal is multiplicatively and additively scaled up and down controlled by the output signal on line 150 of the voltage compensator 270. This means that the switching times $-t_1$ and $-t_2$ are adjusted as in Fig. 3. In return, the phase angle f is controlled.

30 In another alternative embodiment, it is contemplated that output power, rather than voltage alone, may be controlled. For example, lamp power may be regulated for applications such as dimming. The phase angle shift control method described above for voltage regulation may be used for power regulation with the following modifications. The lamp power signal is sensed and fed back to the control circuits. In a preferred embodiment, a

voltage sensing line is positioned at the anode of the lamp L1 to sense lamp voltage. By adding a small resistor in series with the lamp and sensing the voltage across the inserted resistor, lamp current information may be obtained. By further multiplying the sensed lamp voltage and current signal using a standard analog multiplier IC, a feedback signal is produced
5 which is proportional to the lamp power and is fed back to the control circuit compensator. A reference lamp output power is selected. By comparing the feedback signal with the reference power, a compensator provides a phase shift command to the phase shifting circuitry. In such a way, the lamp output power is regulated.

While there has been shown to be what are presently considered to be the
10 preferred embodiments of the invention, it will appear to those of ordinary skill in the art that various modifications can be made without departing from the scope of the invention as defined by the appended claims. Accordingly, the disclosure is illustrative only and not limiting.

CLAIMS:

1. A power supply, which comprises:

a) a resonant circuit (B) having an output voltage and a current oscillating therethrough;

b) a voltage-fed half-bridge inverter (A) producing a source voltage at an output coupled to the resonant circuit, the inverter responsive to a driving signal; and

5 c) a driving circuit (C) producing the driving signal, the driving circuit comprising:

i) voltage compensation circuitry (270) regulating said output voltage with respect to a reference voltage (V_{ref}) and commanding a phase shift angle; and

10 ii) phase-shifting circuitry (208) applying a phase-shift to the sensed current signal, the amount of phase shift commanded by the voltage compensation circuitry (270).

2. A power supply as claimed in claim 1, wherein the driving circuit further

15 comprises circuitry (210) for comparing the phase-shifted current signal with at least one reference.

3. A power supply as claimed in claim 2, wherein the reference is a function of the phase-shift angle.

20

4. A power supply as claimed in claim 2, wherein the circuitry for comparing the phase-shifted current signal with at least one reference comprises a hysteresis relationship.

25

5. A power supply as claimed in claim 2, wherein the driving circuit further comprises means for scaling (R80,R82) the sensed current signal with respect to the voltage signal of the voltage compensator.

6. A power supply as claimed in claim 2, wherein the driving circuit further comprises means for adding (370,270) the sensed current signal with the output signal of the voltage compensator.

5 7. A power supply, which comprises:

- a) a resonant circuit (B) having an output voltage, an output power, and a current oscillating therethrough;
- b) a voltage-fed half-bridge inverter (A) producing a source voltage at an output coupled to the resonant circuit, the inverter responsive to a driving signal; and
- 10 c) a driving circuit (C) producing the driving signal, the driving circuit comprising:
 - i) power compensation circuitry (270) regulating said output power with respect to a reference power signal and commanding a phase shift angle; and
 - ii) phase-shifting circuitry (208) applying a phase-shift to the sensed current signal, the amount of phase shift commanded by the power compensation circuitry.

15 8. A method for switching a power supply, which comprises:

providing a resonant circuit (B) having a current oscillating therethrough and an output voltage;

20 providing an inverter (A) responsive to a driving signal and producing a voltage at an output coupled to the resonant circuit;

detecting the output voltage and comparing the output voltage with a reference voltage;

25 commanding a phase-angle shift to reduce the difference between the output voltage and the reference voltage;

applying the phase-angle shift to a signal representing the current oscillating through the resonant circuit and producing a phase-shifted current signal; driving the inverter based upon the phase-shifted current signal.

30 9. A method for switching a power supply as claimed in claim 8, wherein the step of driving the inverter further comprises:

comparing the phase-shifted current signal with a hysteresis threshold.

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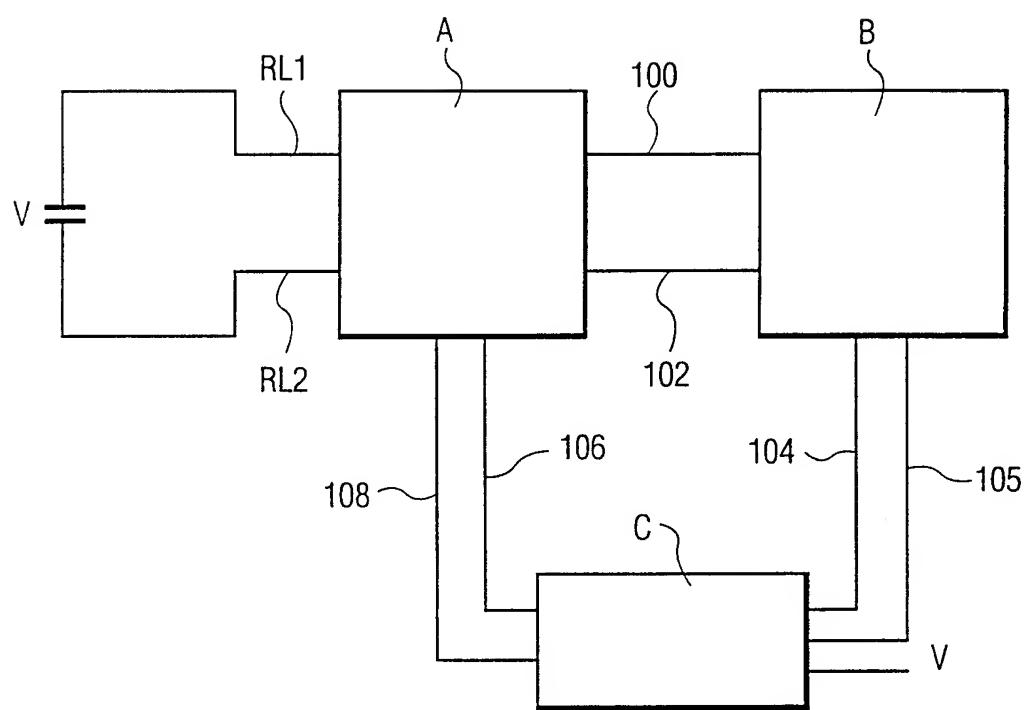


FIG. 1

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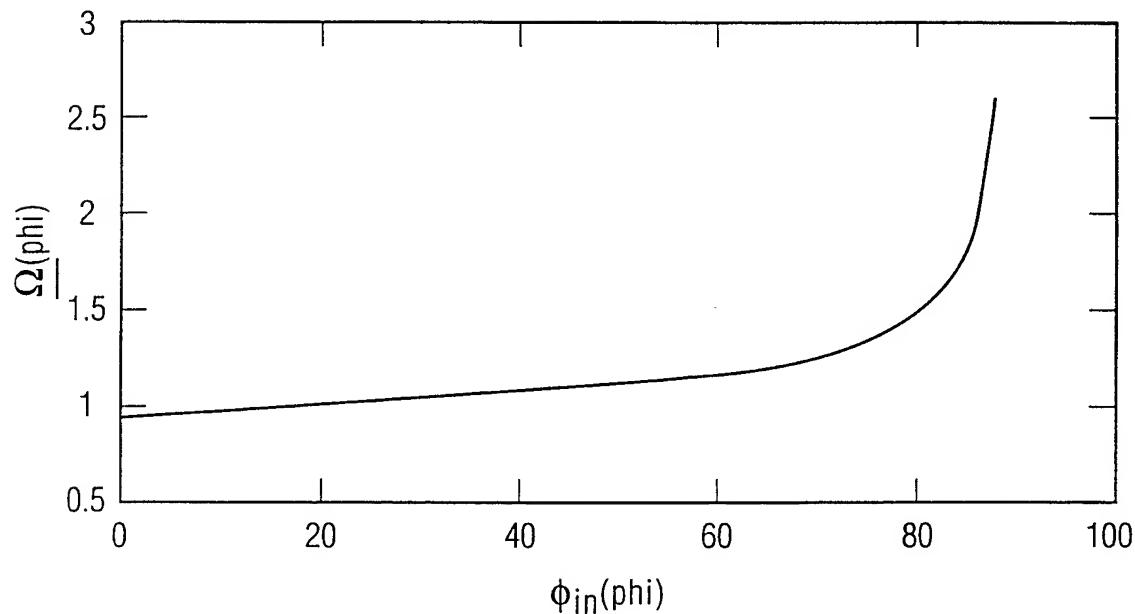


FIG. 2A

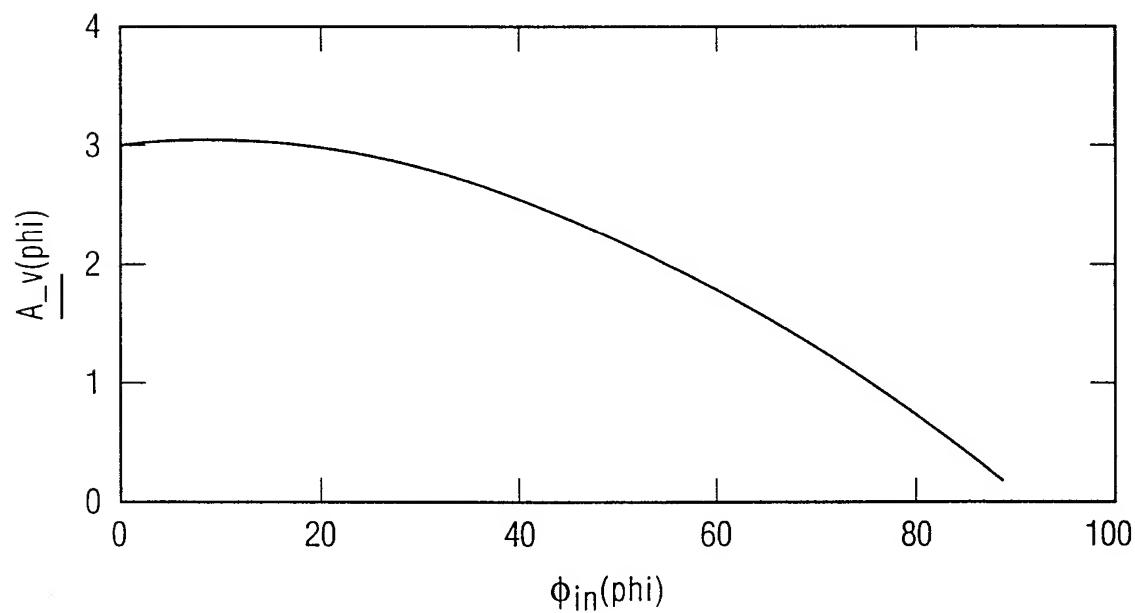


FIG. 2B

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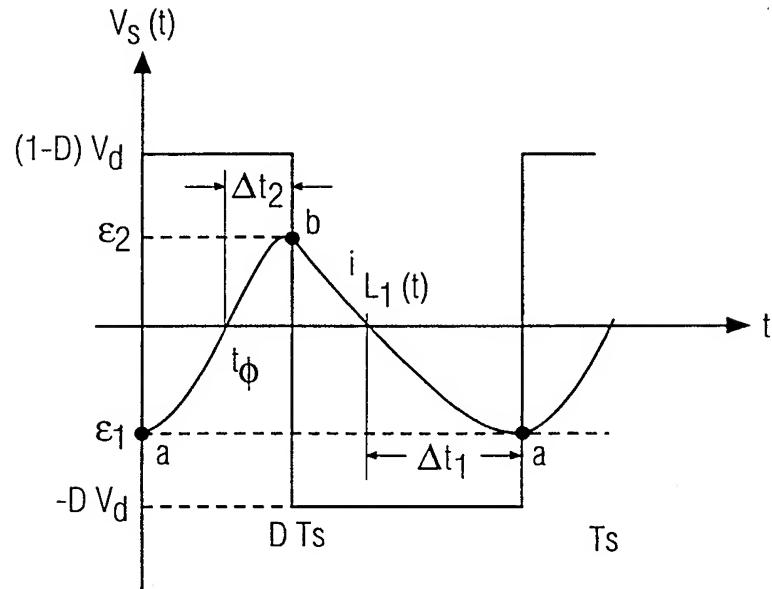


FIG. 3

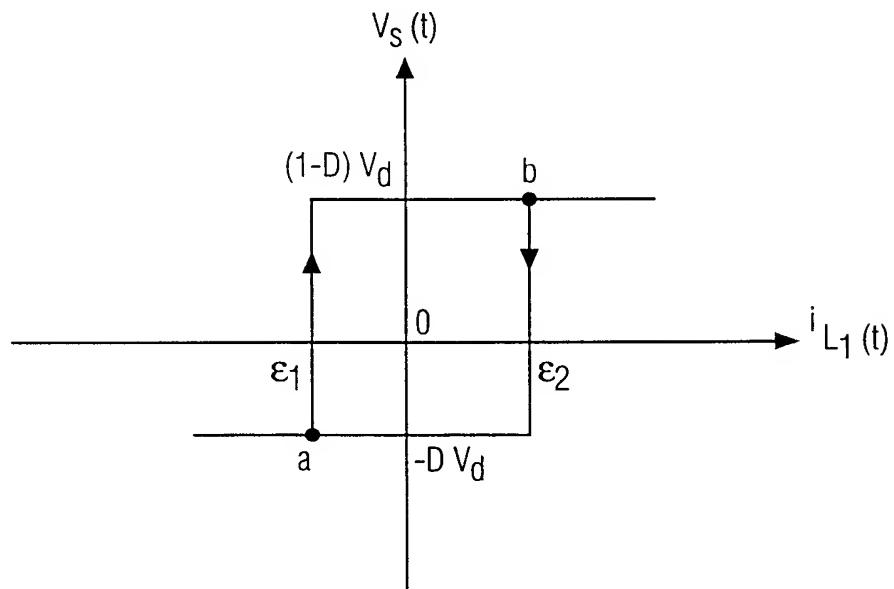


FIG. 6

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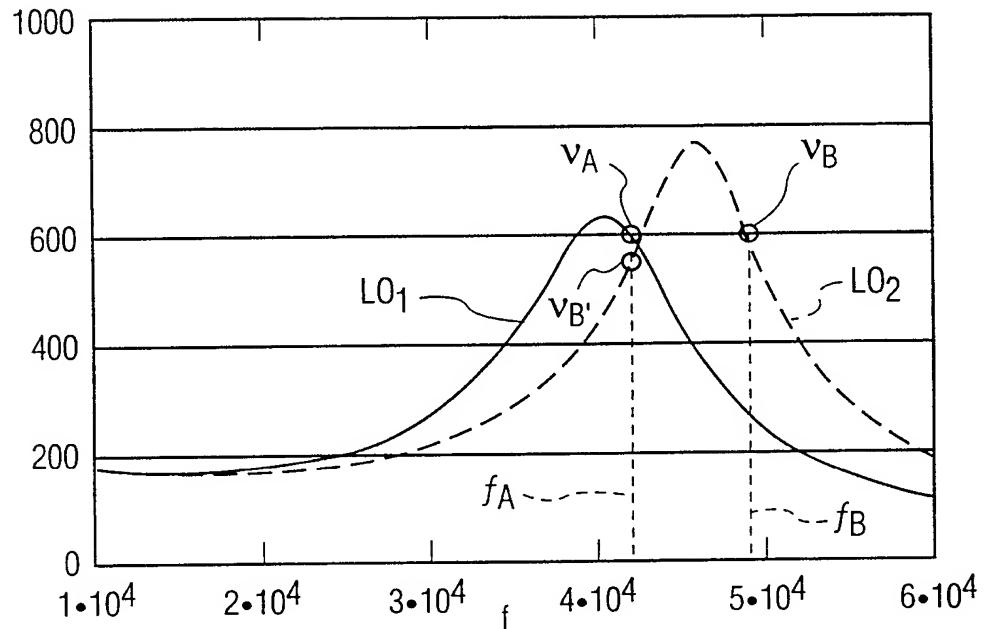


FIG. 4A

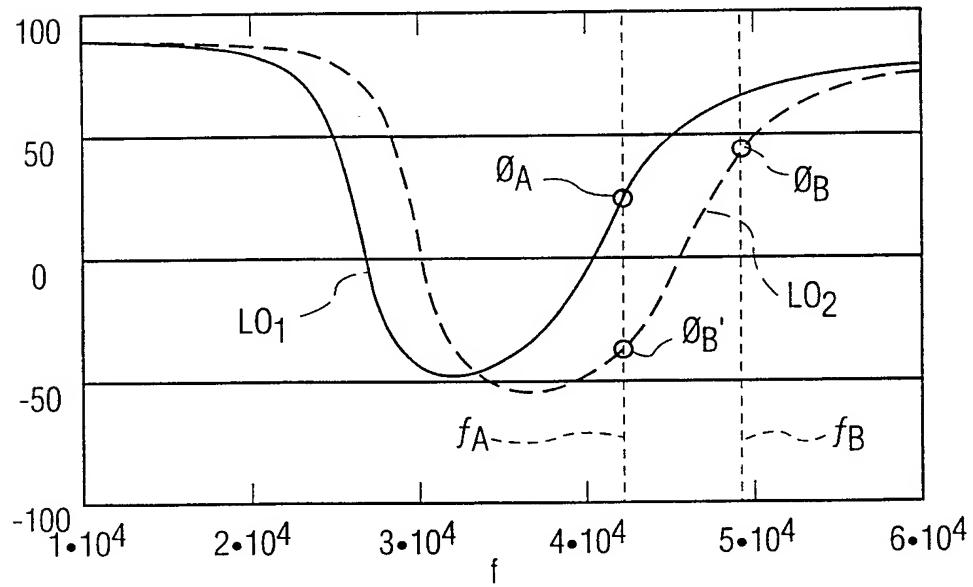


FIG. 4B

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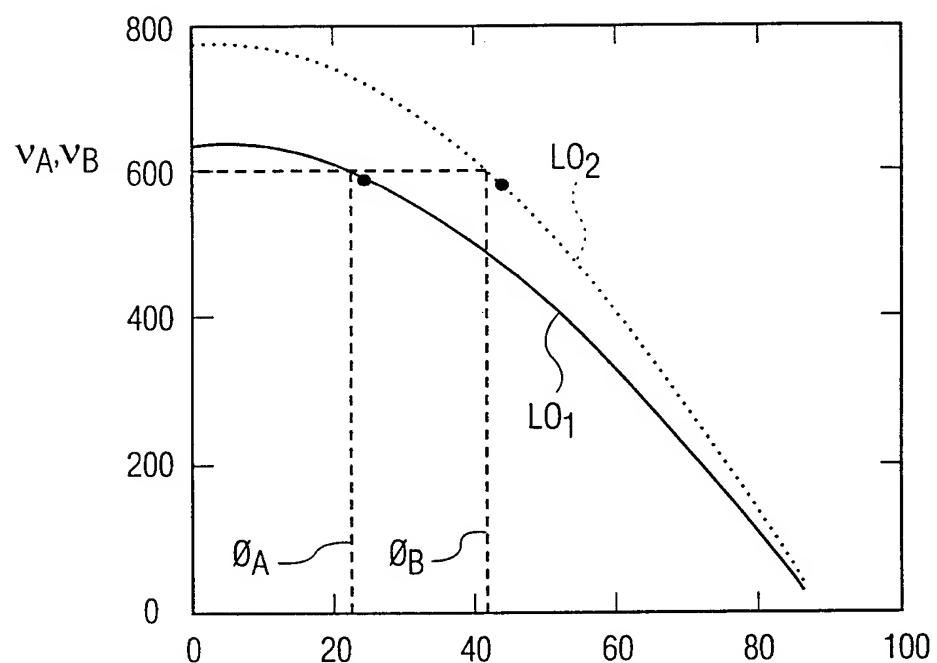
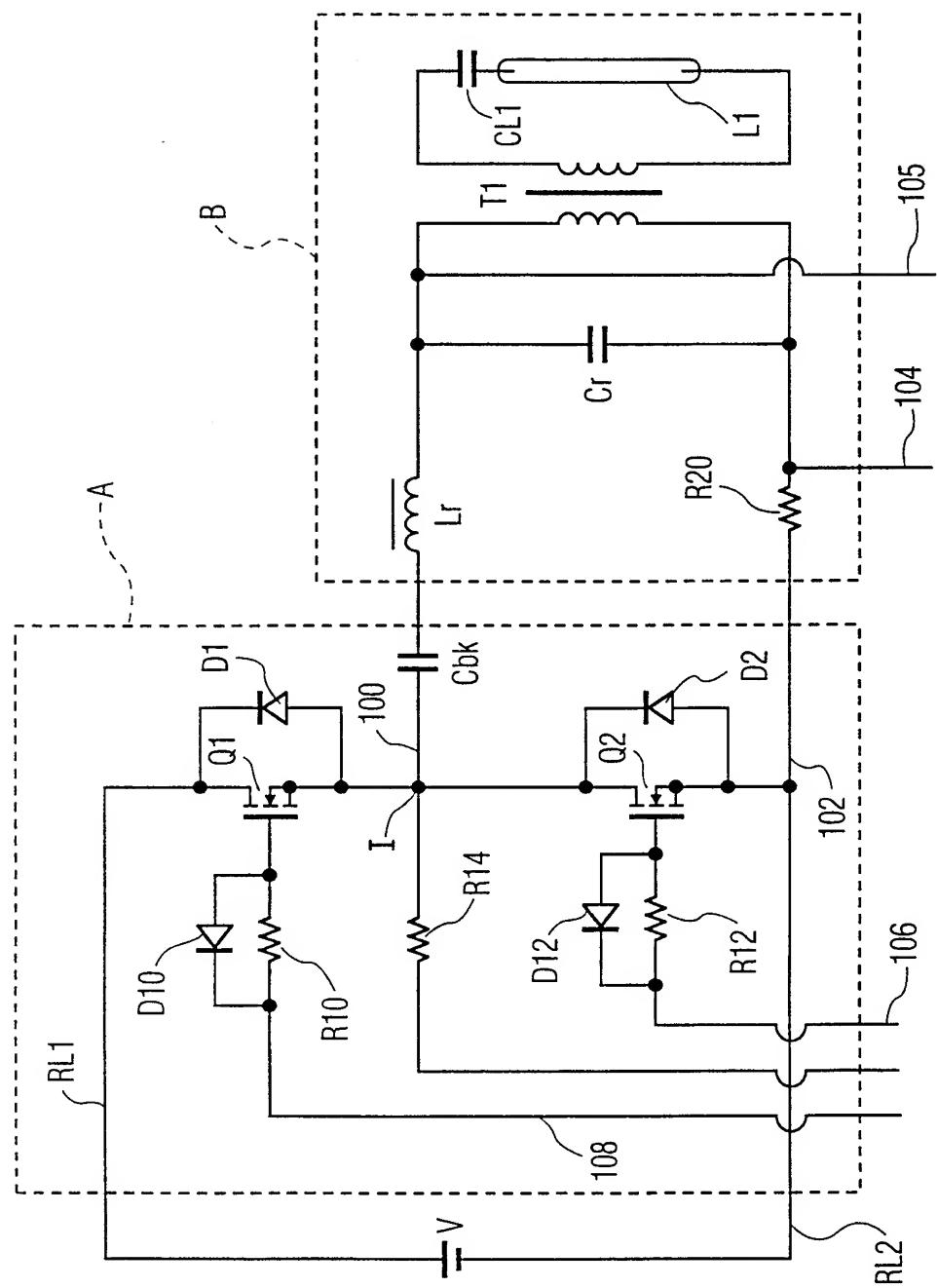


FIG. 5

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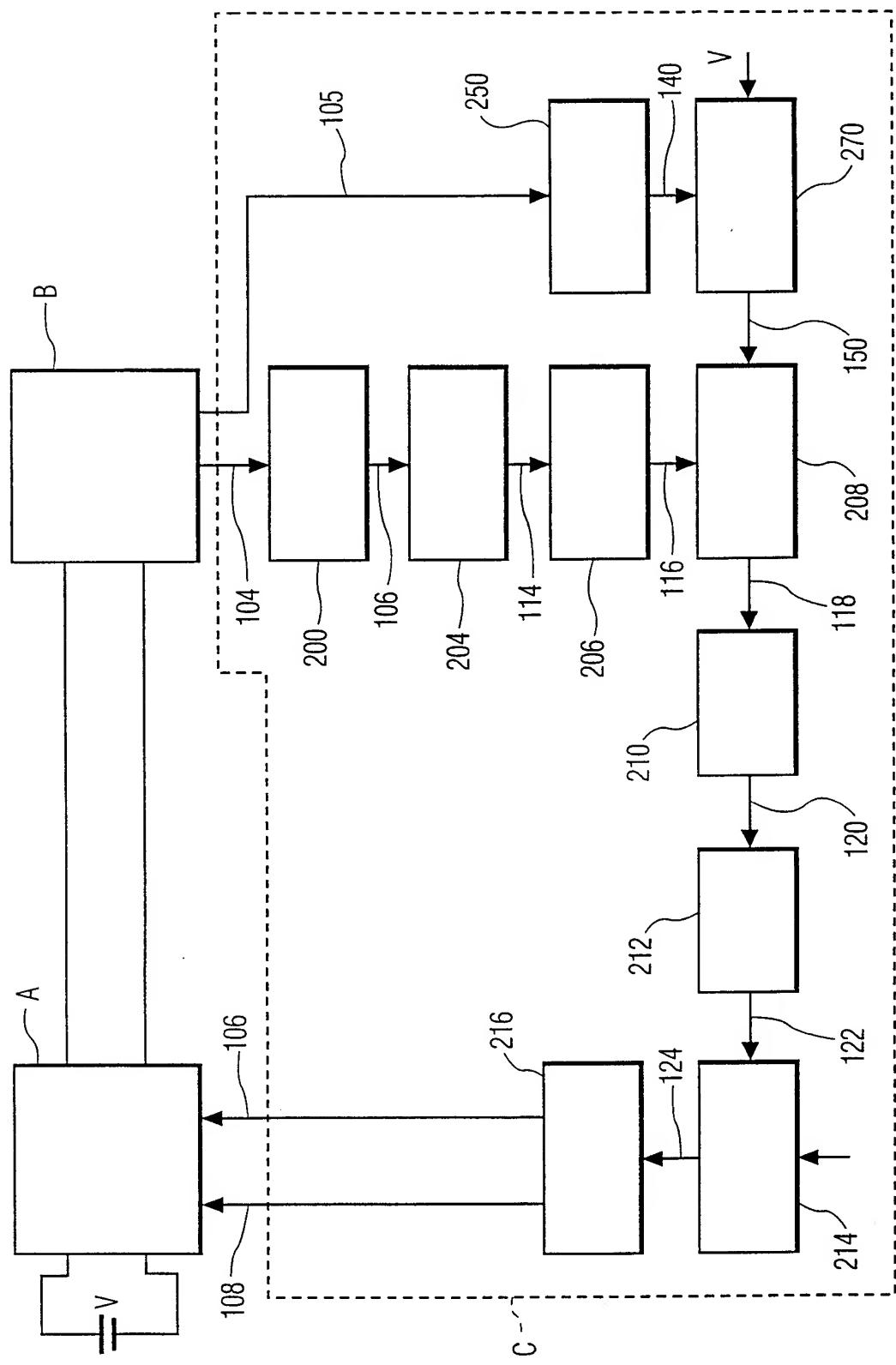


FIG. 8

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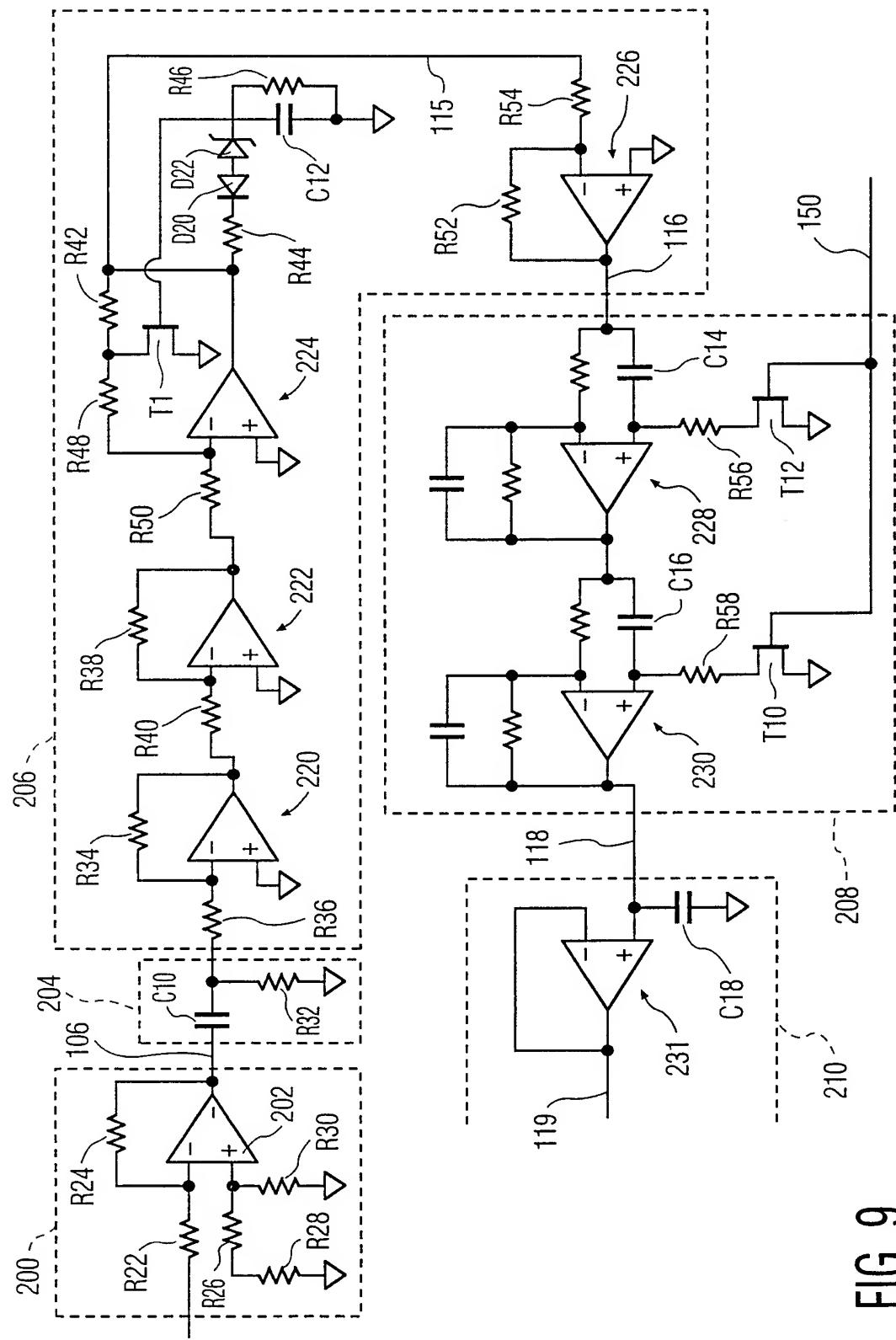


FIG. 9

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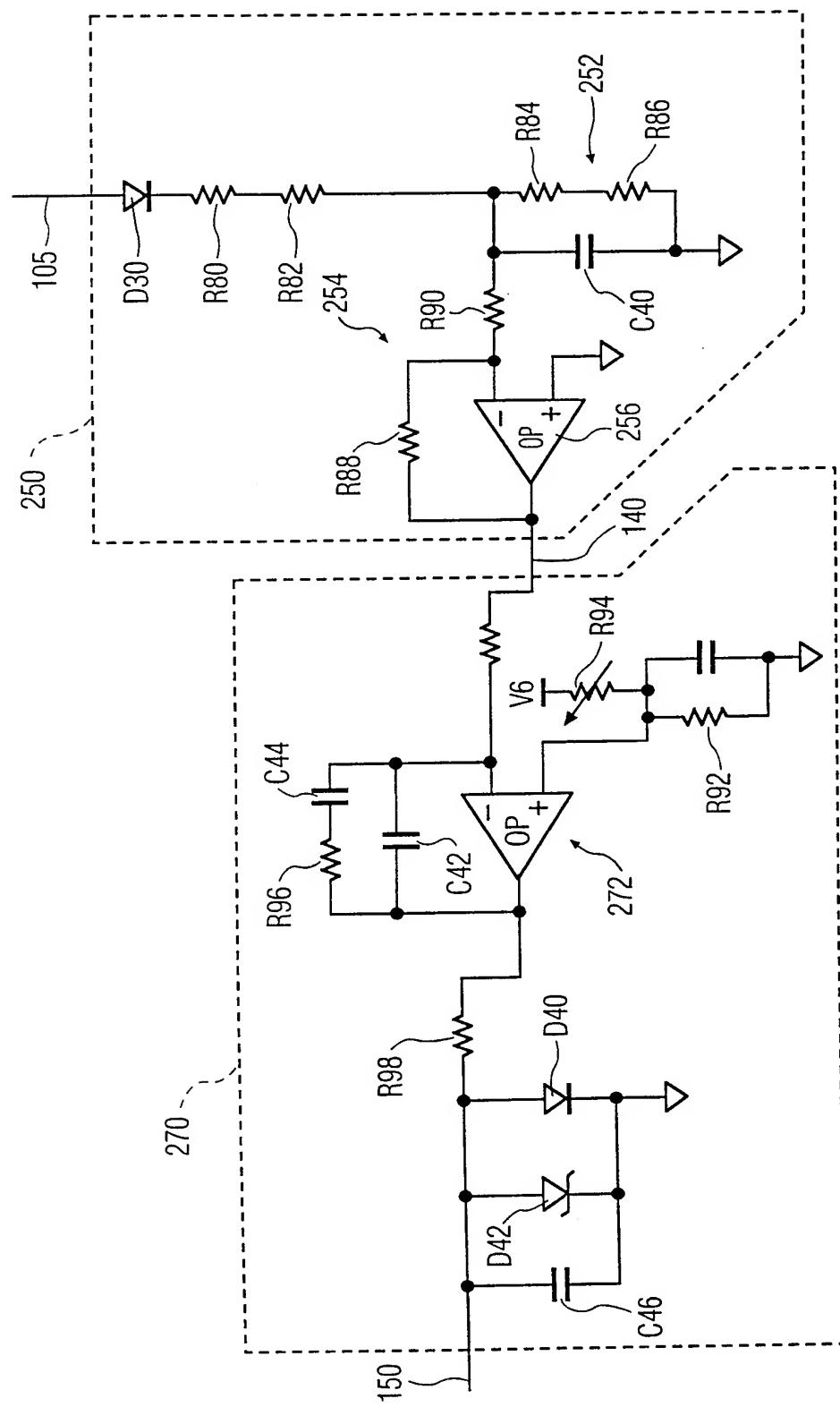


FIG. 9A

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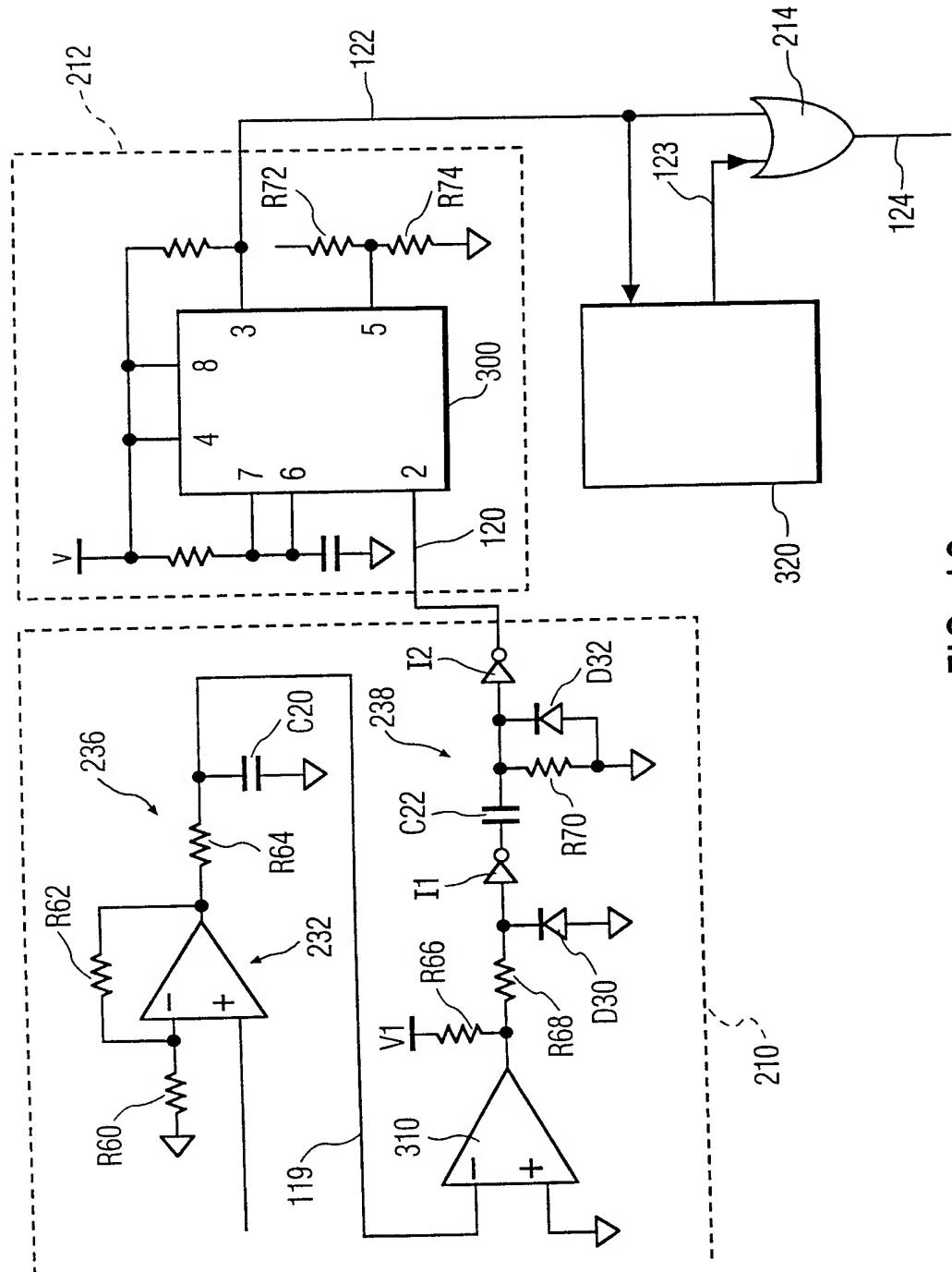


FIG. 10

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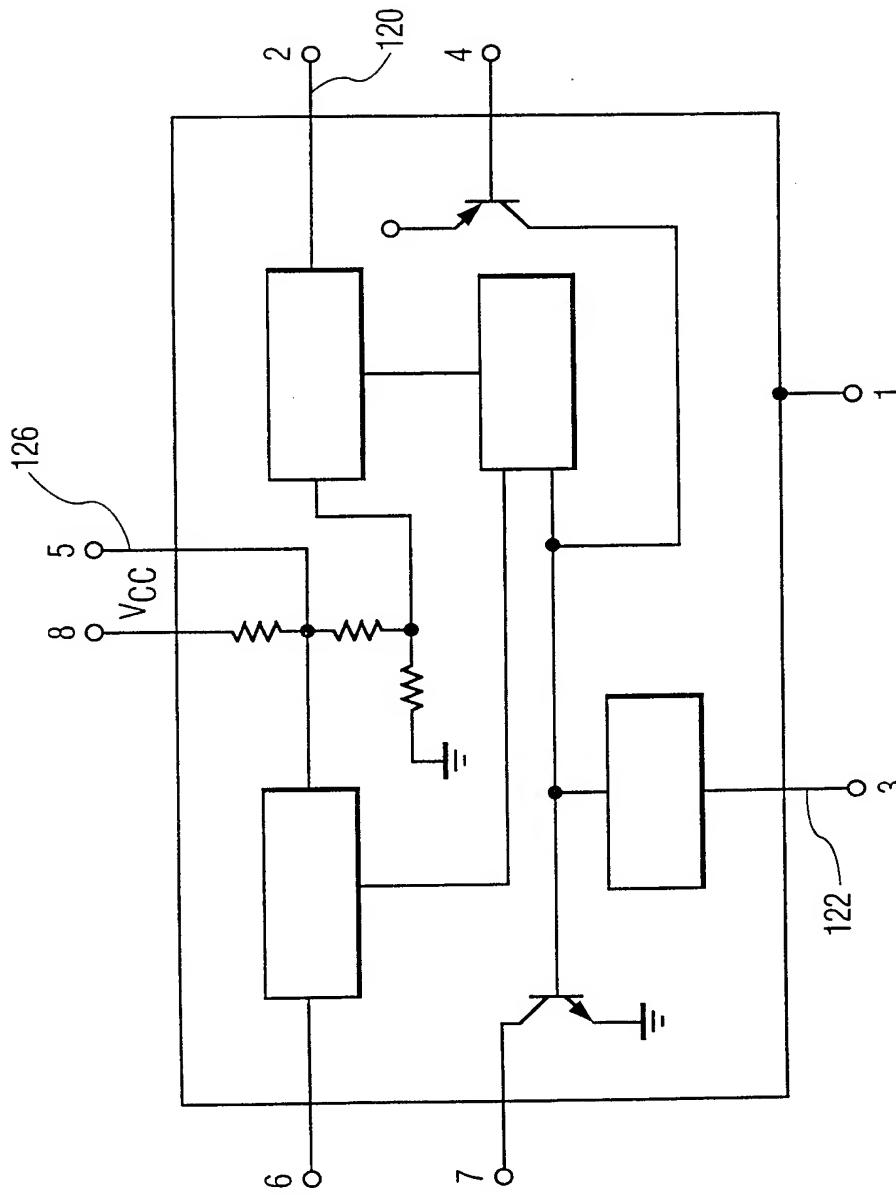


FIG. 10A

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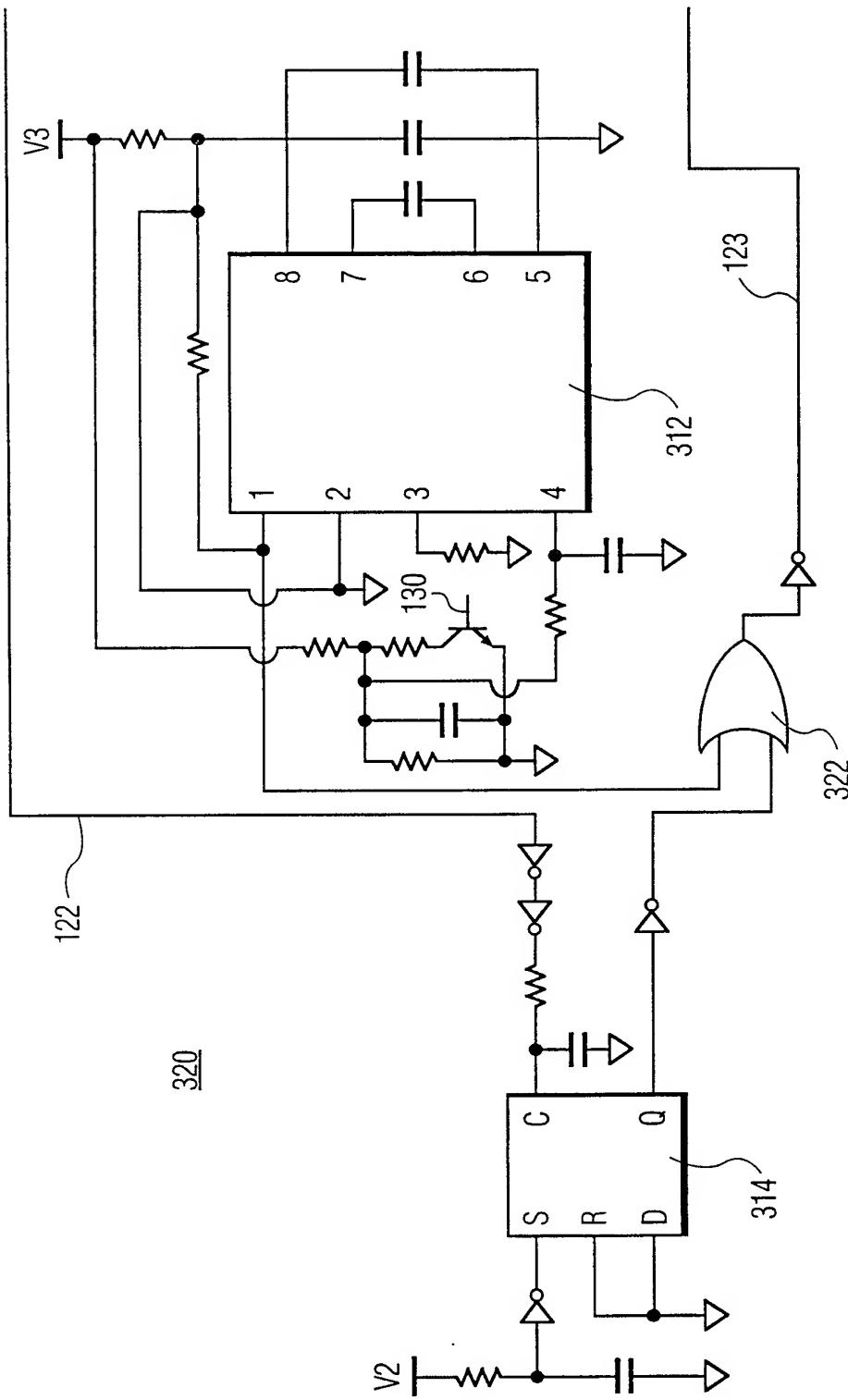


FIG. 11

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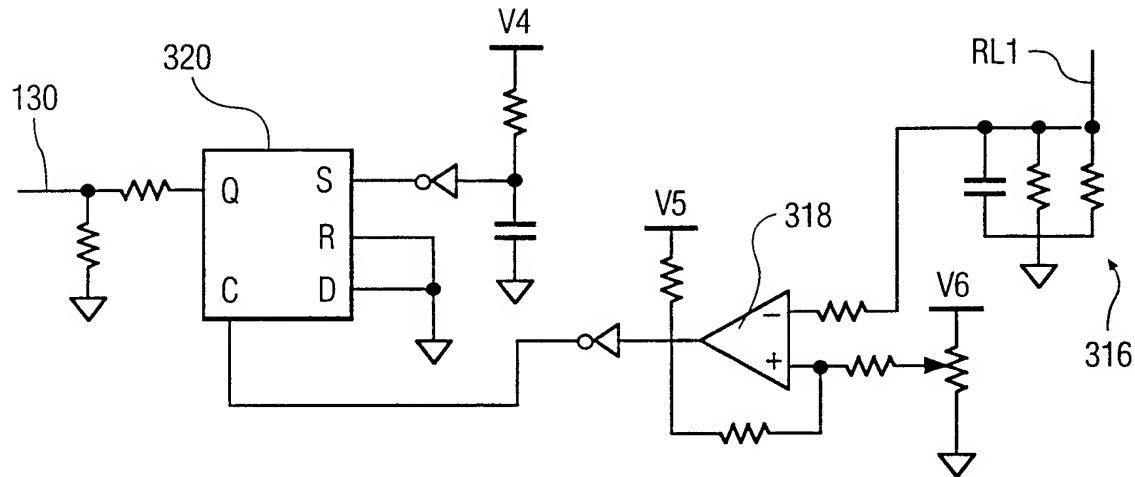


FIG. 12

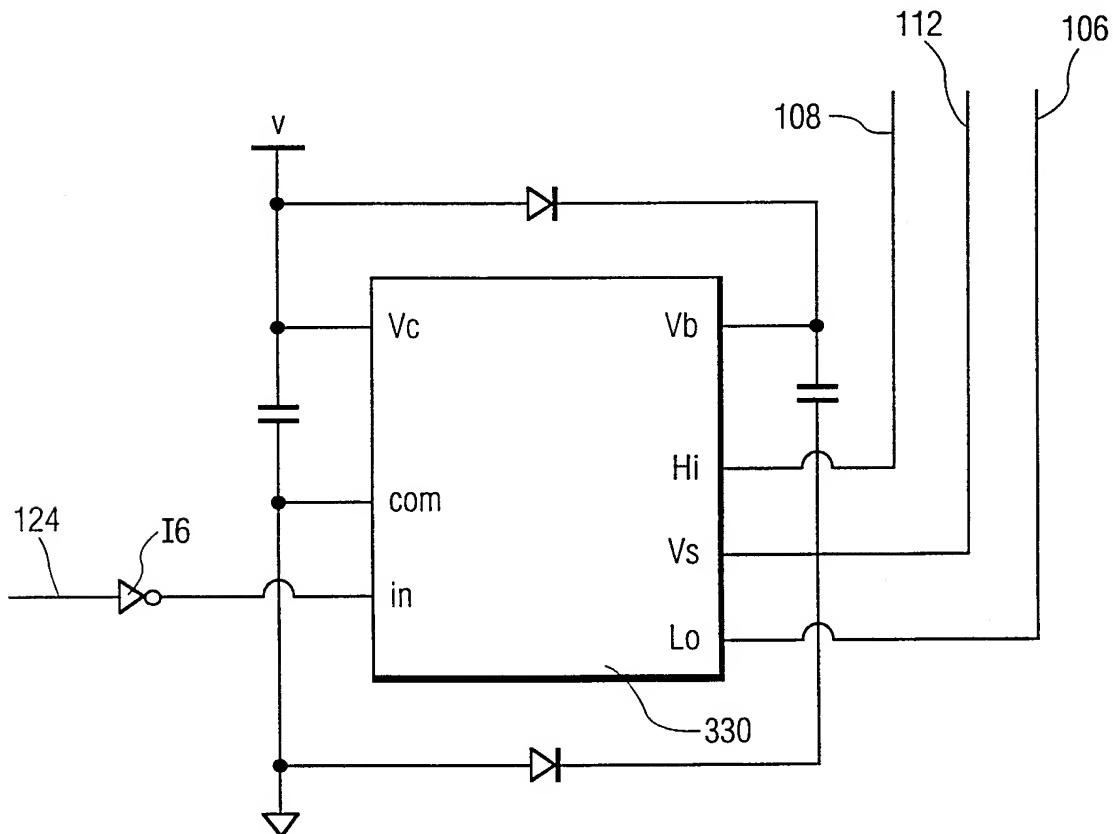


FIG. 13

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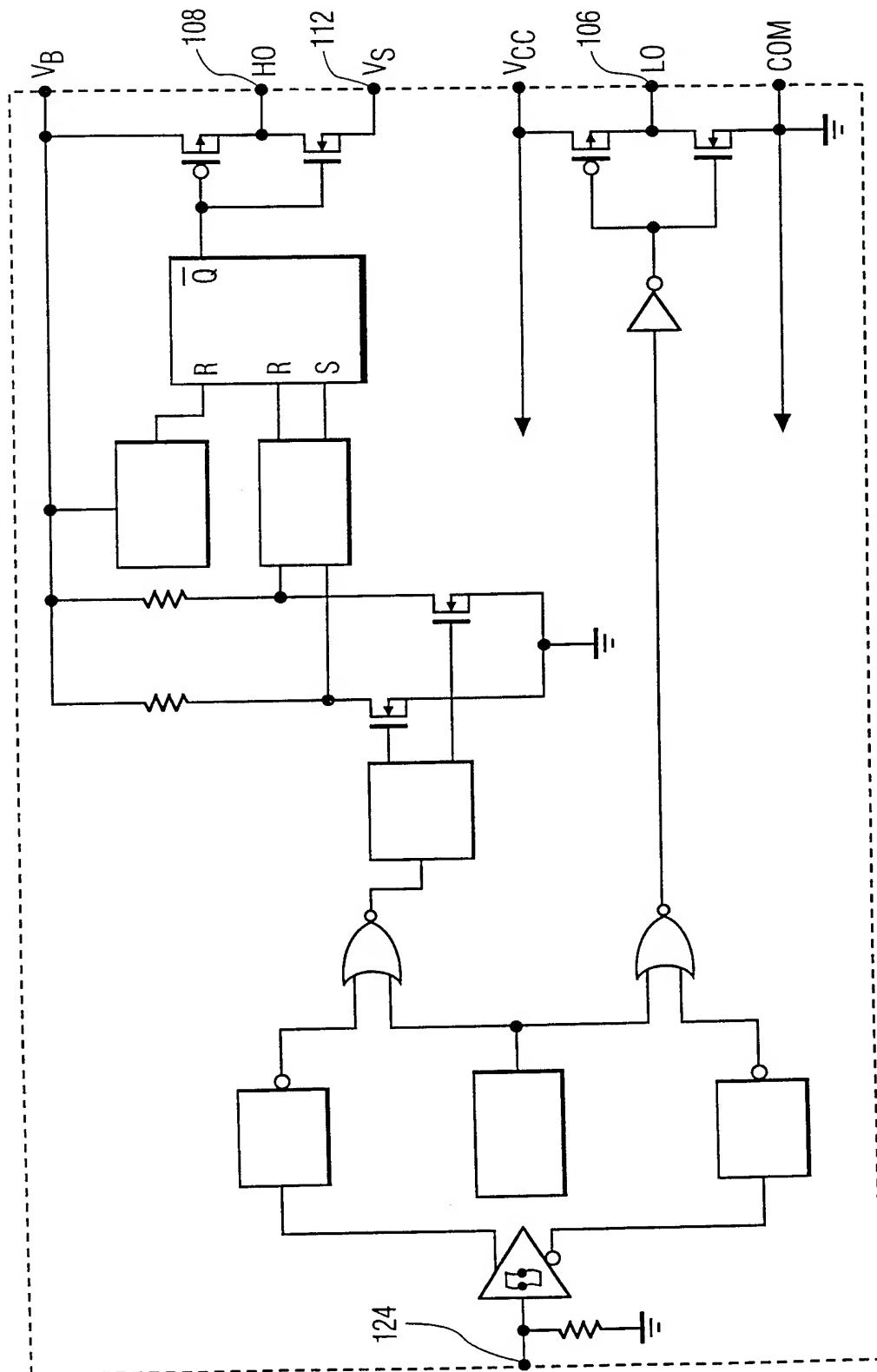


FIG. 13A

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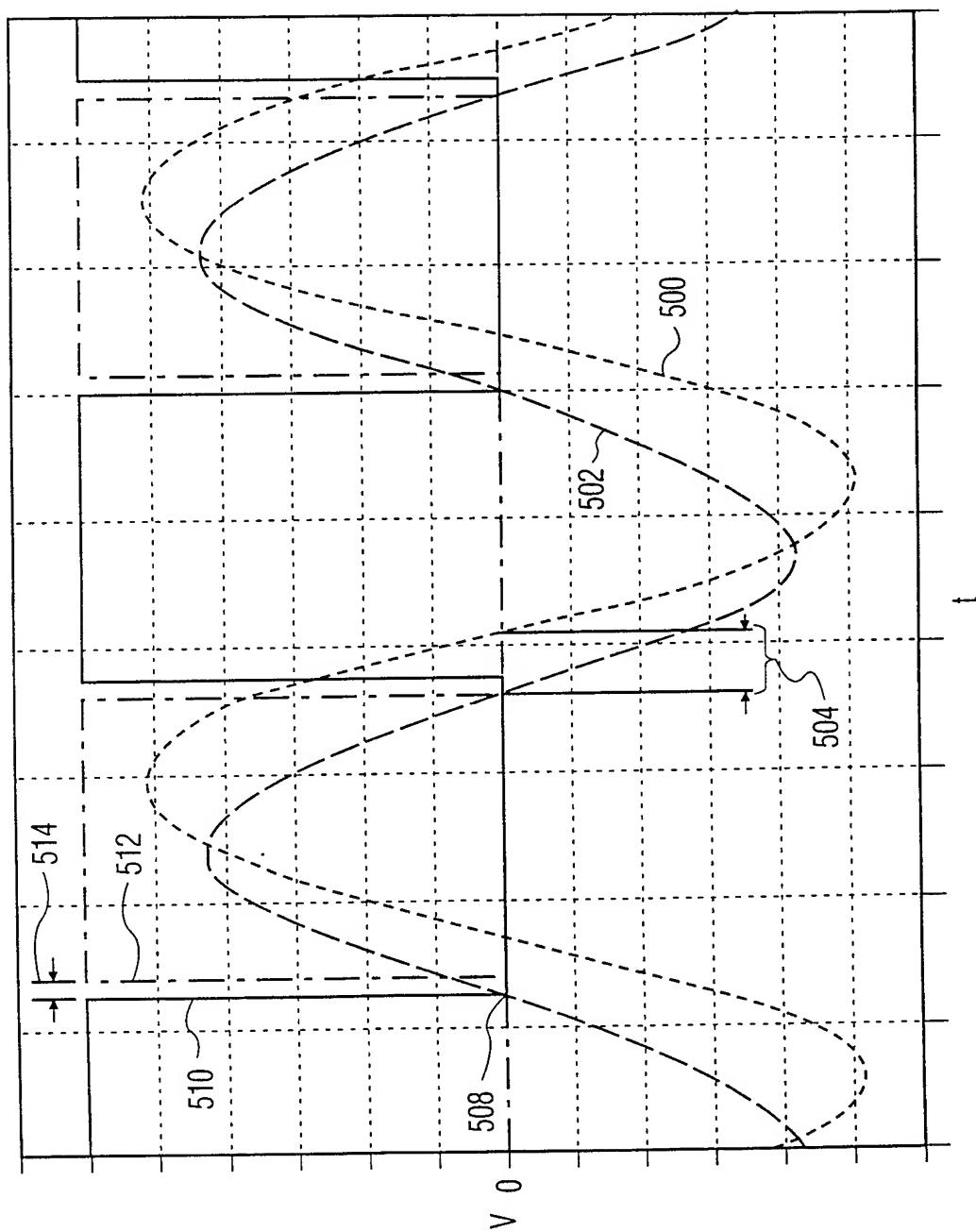


FIG. 14

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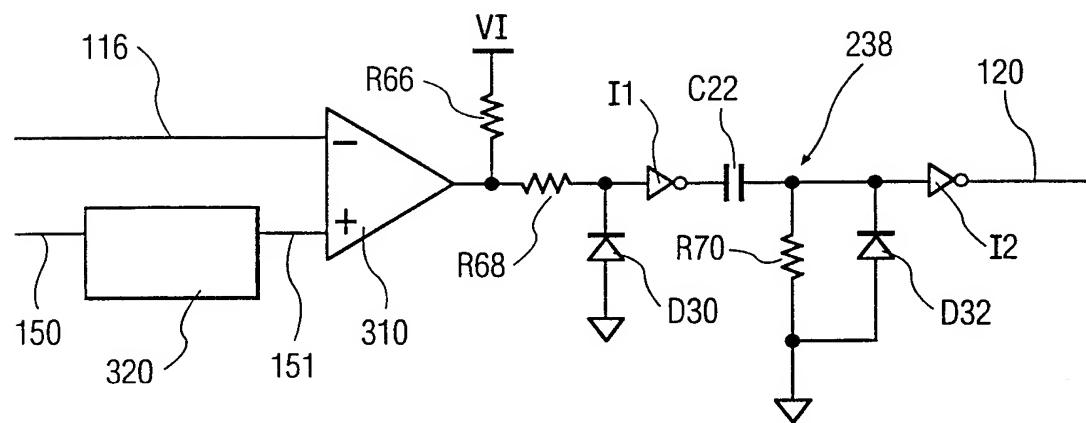


FIG. 15

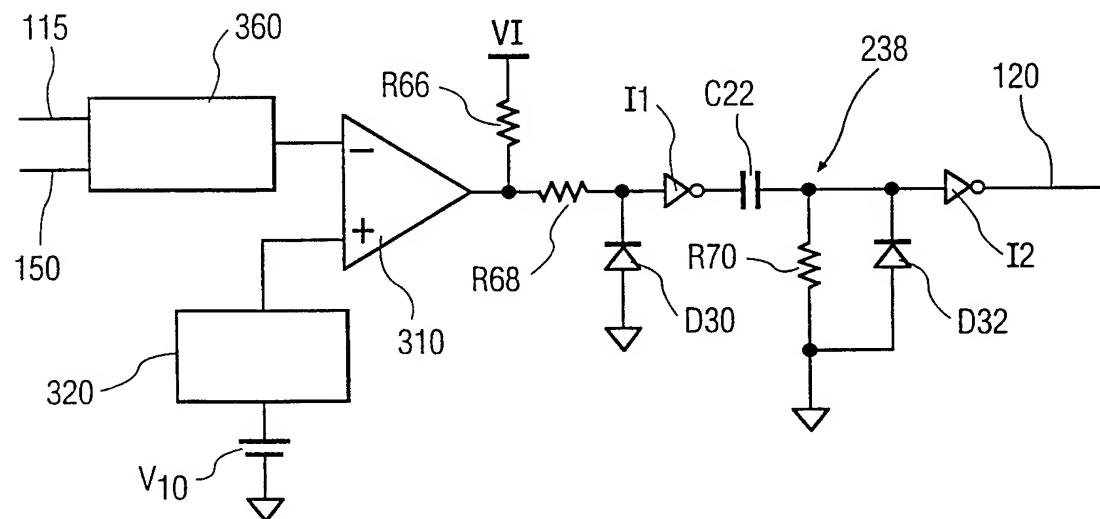


FIG. 16

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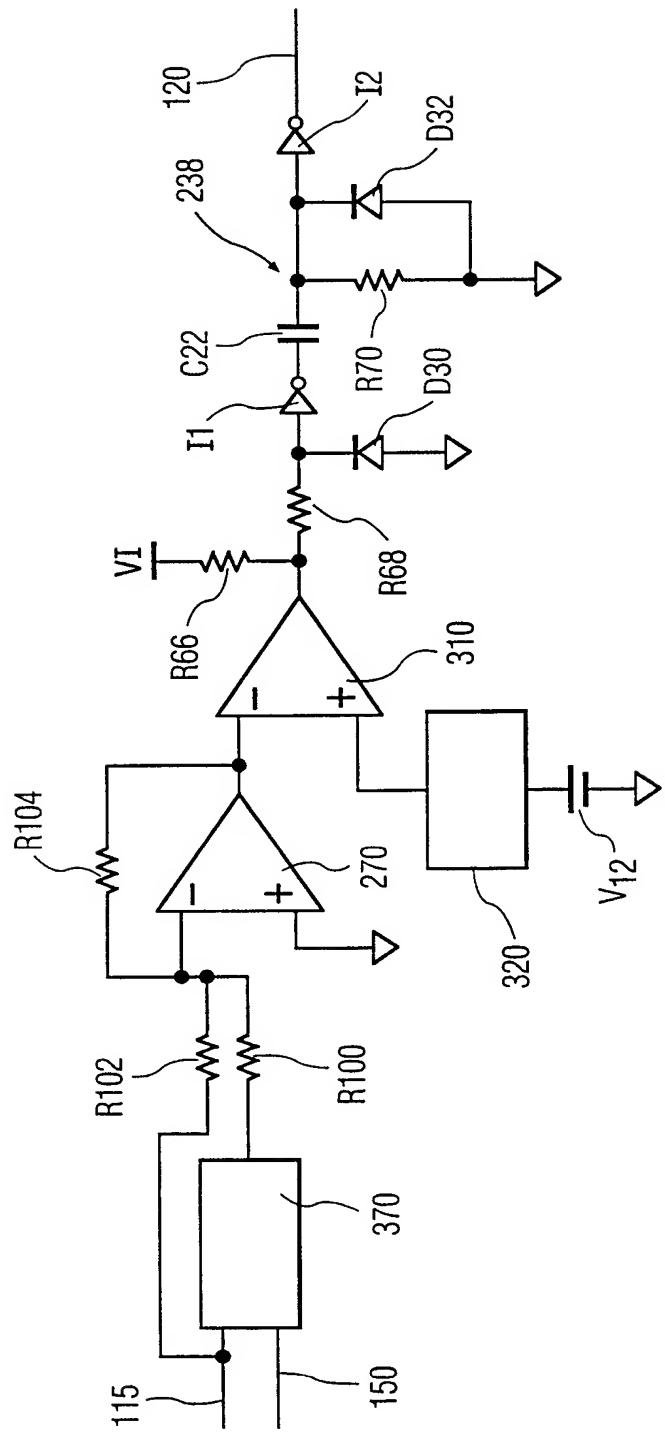


FIG. 17